HC2323

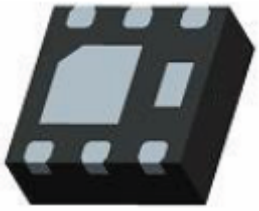
12V P-Channel MOSFET

General Description

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

V_{DS}	-12V
I_D (at V_{GS}=-4.5V)	-16A
$R_{DS(ON)}$ (at V_{GS}=-4.5V)	12mΩ(Typ)



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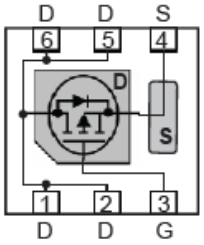
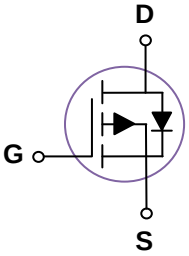


Pin configuration (Top view)



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-12	V
Gate-Source Voltage		V_{GS}	±10	V
Drain Current-Continuous	TC=25°C	I_D	-16	A
	TC=100°C	I_D	-10	A
Maximum Power Dissipation		P_D	18	W
Drain Current – Pulsed1		I_{DM}	-65	A
Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	℃

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance junction-case	$R_{\theta Jc}$		38	℃ /W
Thermal Resistance junction-to-Ambient	$R_{\theta JA}$		80	℃ /W

Electrical Characteristics (TJ=25℃ unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=-250μA	-12			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-12V,V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±12V,V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250μA	-0.4	-0.7	-1.0	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=-4.5V, I_D=-6.7A		12	15	mΩ
		V_{GS}=-2.5V, I_D=-6.2A		16	23	mΩ
DYNAMIC PARAMETERS						
Ciss	Input Capacitance	V_{DS}=-10V,V_{GS}=0 V, F=1.0MHz		2700		pF
C_{oss}	Output Capacitance			680		pF
C_{rss}	Reverse Transfer Capacitance			590		pF
SWITCHING PARAMETERS						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=-6V,I_D=-1A , V_{GS}=-4.5V, R_G=10Ω		11		nS
t_r	Turn-on Rise Time			35		nS
$t_{d(off)}$	Turn-Off Delay Time			30		nS
t_f	Turn-Off Fall Time			10		nS
Q_g	Total Gate Charge	V_{DS}=-6V,I_D=-10 A, V_{GS}=-4.5V		35		nC
Q_{gs}	Gate-Source Charge			5		nC
Q_{gd}	Gate-Drain Charge			10		nC
V_{SD}	Diode Forward Voltage	V_{GS}=0V,I_{SD}=-1A		0.72	1.4	V
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, F=1MHz		4		Ω

Note：

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
3. Essentially independent of operating temperature.

Typical Performance Characteristics

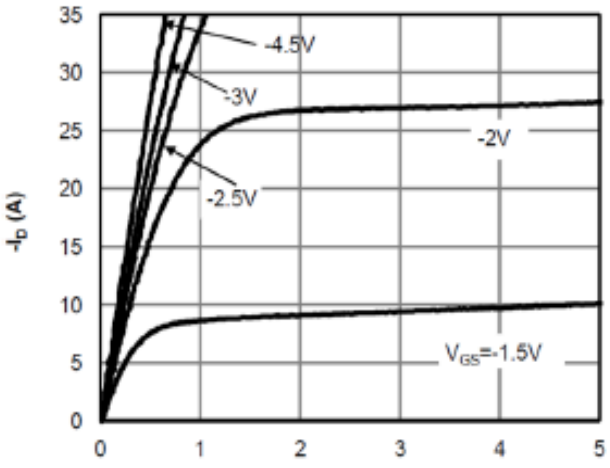


Fig 1: On-Region Characteristics

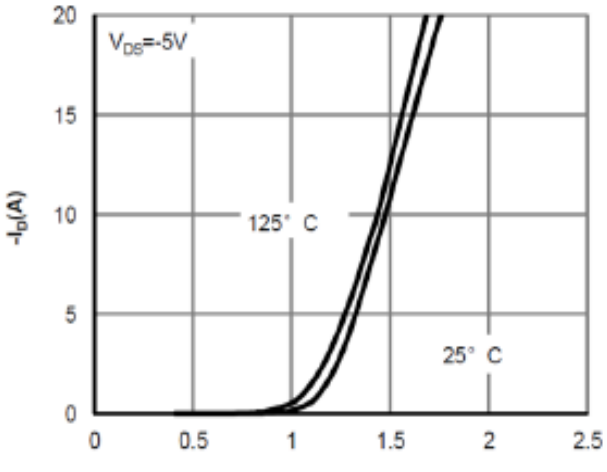


Figure 2: Transfer Characteristics

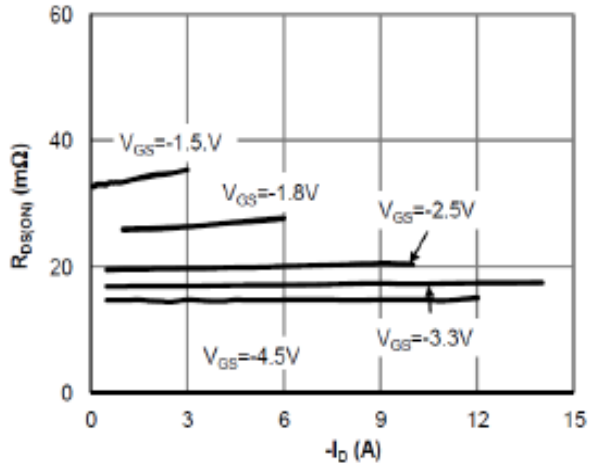


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

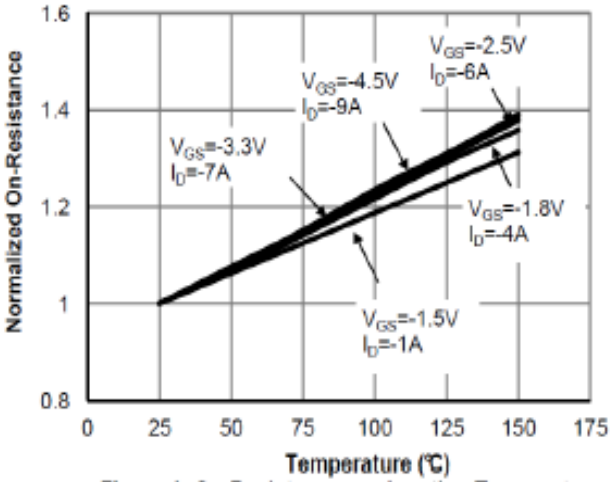


Figure 4: On-Resistance vs. Junction Temperature

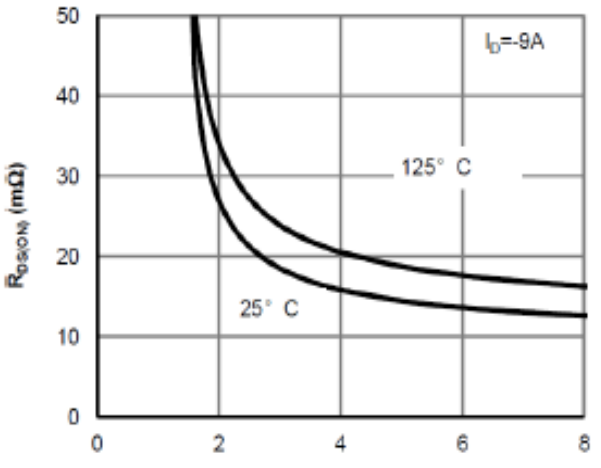


Figure 5: On-Resistance vs. Gate-Source Voltage

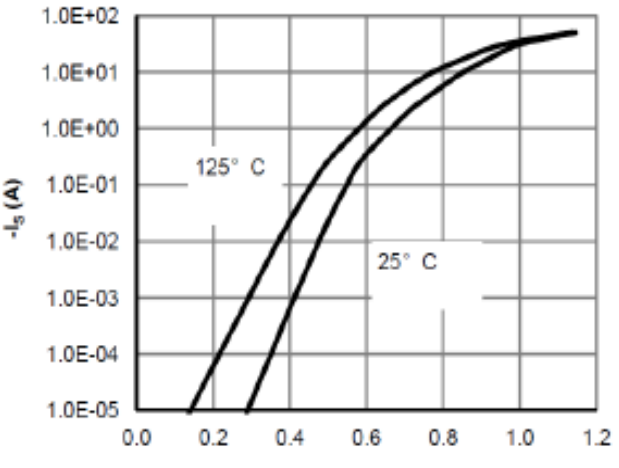


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

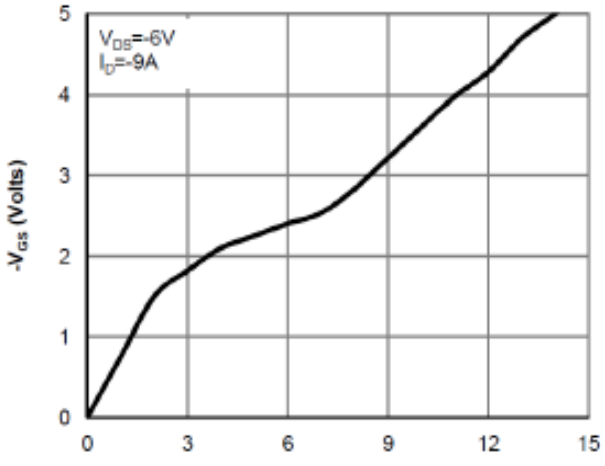


Figure 7: Gate-Charge Characteristics

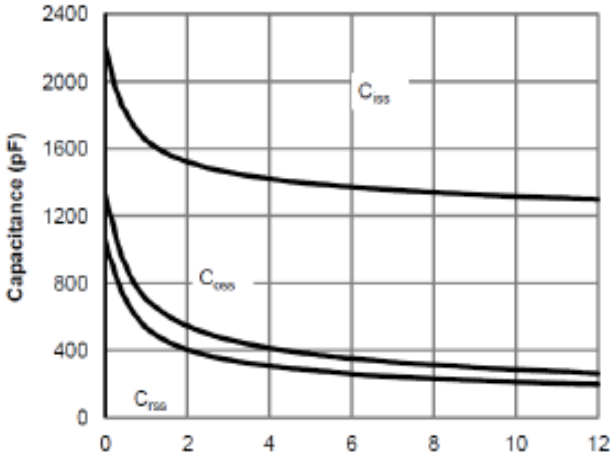


Figure 8: Capacitance Characteristics

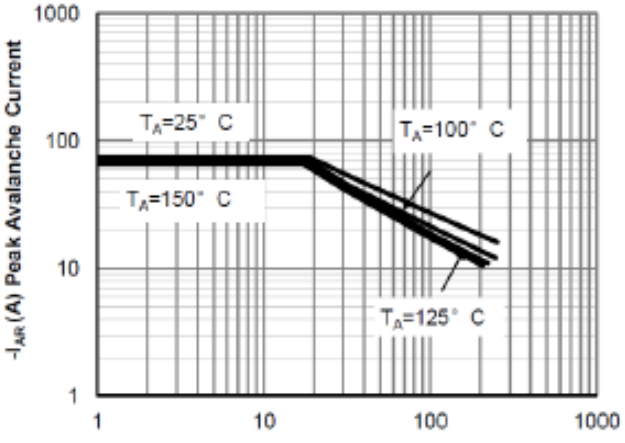


Figure 9: Single Pulse Avalanche capability

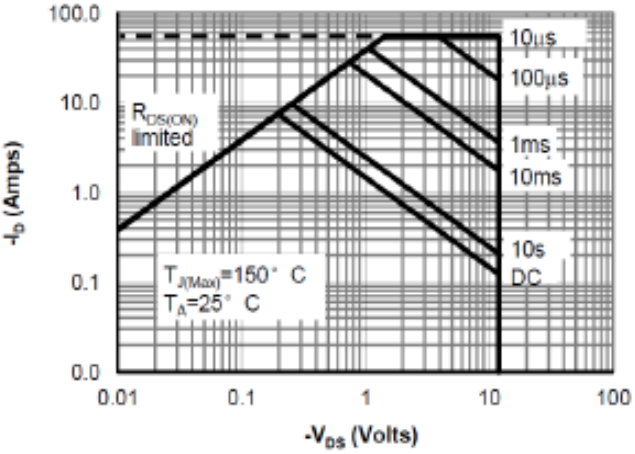


Figure 10: Maximum Forward Biased Safe Operating Area

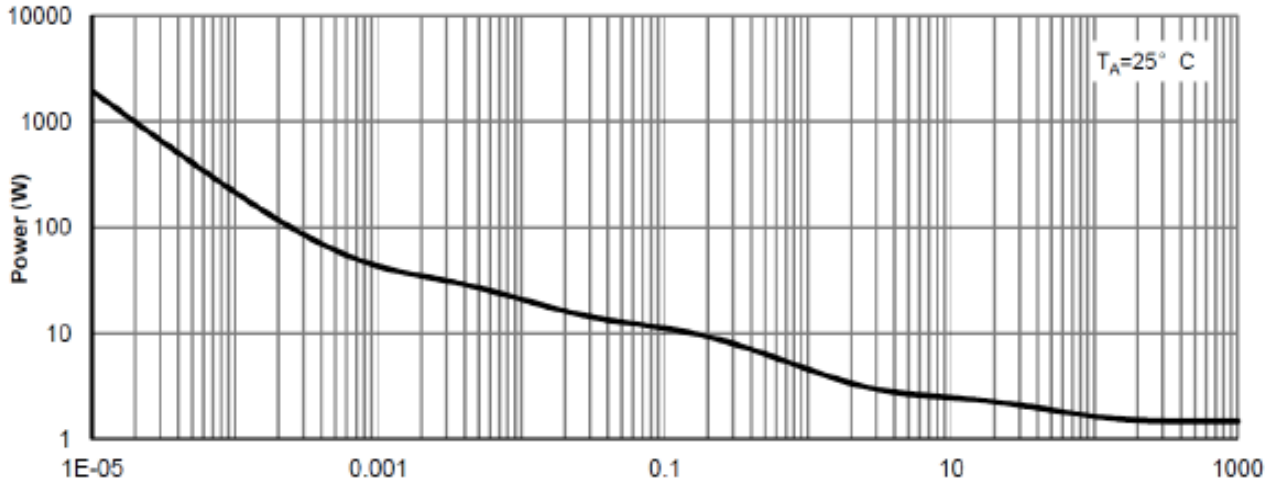
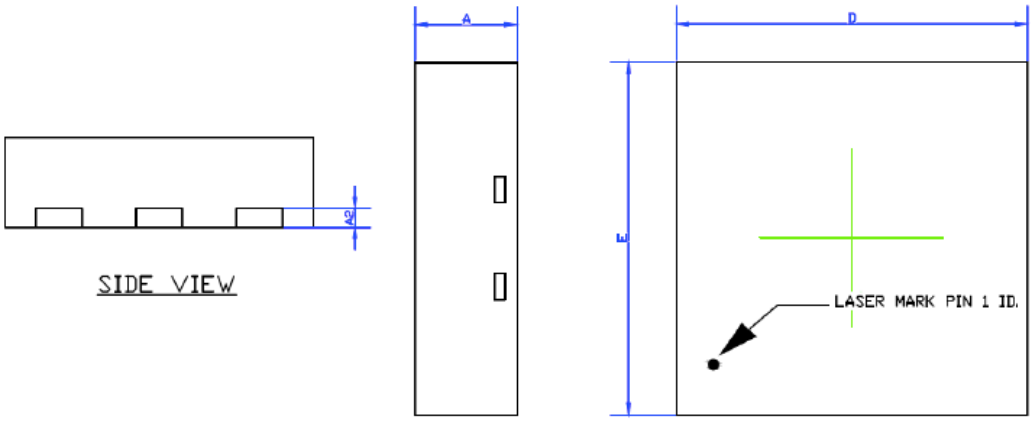


Figure 11: Single Pulse Power Rating Junction-to-Ambient

DFN2020-6L PACKAGE INFORMATION

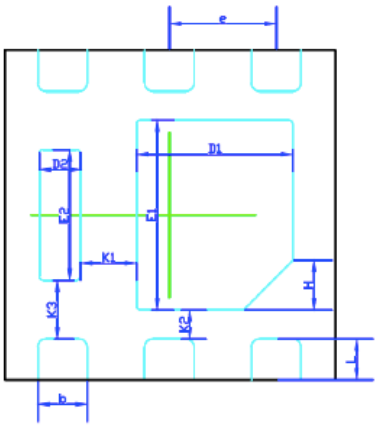


SIDE VIEW

SIDE VIEW

TOP VIEW

COMMON DIMENSION (MM)			
PKG	DFN2020-6L-4		
SYMBOL	MIN.	NOM.	MAX
A	0.527	0.552	0.577
A2		0.127REF	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D1	0.85	0.95	1.05
E1	1.05	1.15	1.25
D2	0.20	0.25	0.30
E2	0.69	0.79	0.89
e	0.55	0.65	0.75
H	0.25	0.30	0.35
K1	0.25MIN		
K2	0.15MIN		
K3	0.20MIN		
L	0.20	0.25	0.30



BOTTOM VIEW