

General Description

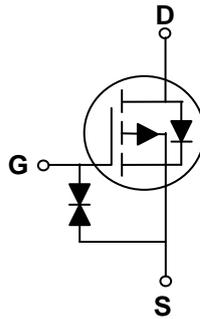
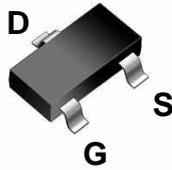
These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

V_{DS}	-20V
I_D (at $V_{GS}=-4.5V$)	-0.5A
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	580mΩ(Typ)

ESD Protected Up to 2.0KV (HBM)

SOT323



Absolute Maximum Ratings $T_A=25^{\circ}C$ unless otherwise noted

Parameter	Symbol	Maximum	Units	
Drain-Source Voltage	V_{DS}	-20	V	
Gate-Source Voltage	V_{GS}	±12	V	
Drain Current-Continuous	TC=25°C	I_D	-0.5	A
	TC=100°C	I_D	-0.4	A
Maximum Power Dissipation	P_D	0.18	W	
Drain Current – Pulsed1	I_{DM}	-2.6	A	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C	

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance junction-to-solder point	$R_{\theta JSP}$		40	°C /W
Thermal Resistance junction-to-Ambient	$R_{\theta JA}$		830	°C /W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-20V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±10V, V _{DS} =0V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-0.3	-0.6	-1.2	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =-4.5V, I _D =-0.5A		580	850	mΩ
		V _{GS} =-2.5V, I _D =-0.3A		850	1200	mΩ
		V _{GS} =-1.8V, I _D =-0.2A		1350	2000	mΩ
I _S	Maximum Body-Diode Continuous Current				-0.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{DS} =-10V, V _{GS} =0V, F=1.0MHz		71		pF
C _{oss}	Output Capacitance			20		pF
C _{rss}	Reverse Transfer Capacitance			15		pF
SWITCHING PARAMETERS						
t _{d(on)}	Turn-on Delay Time	V _{DD} =-10V, I _D =-0.2A, V _{GS} =-4.5V, R _G =10Ω		4		nS
t _r	Turn-on Rise Time			19		nS
t _{d(off)}	Turn-Off Delay Time			16		nS
t _f	Turn-Off Fall Time			25		nS
Q _g	Total Gate Charge	V _{DS} =-10V, I _D =-0.2A, V _{GS} =-4.5V		1.2		nC
Q _{gs}	Gate-Source Charge			0.37		nC
Q _{gd}	Gate-Drain Charge			0.27		nC
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _{SD} =-1A		0.7	1.2	V

Note:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
3. Essentially independent of operating temperature.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

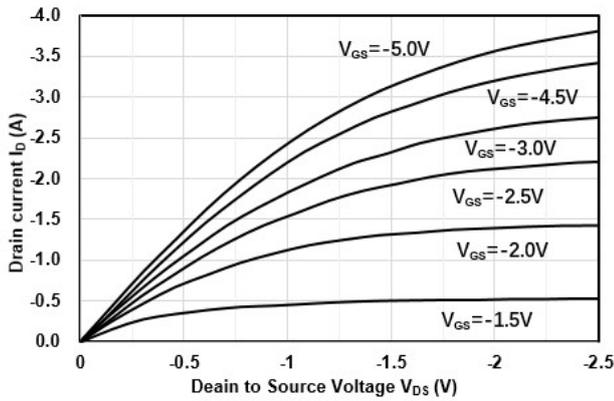


Figure1. Output Characteristics

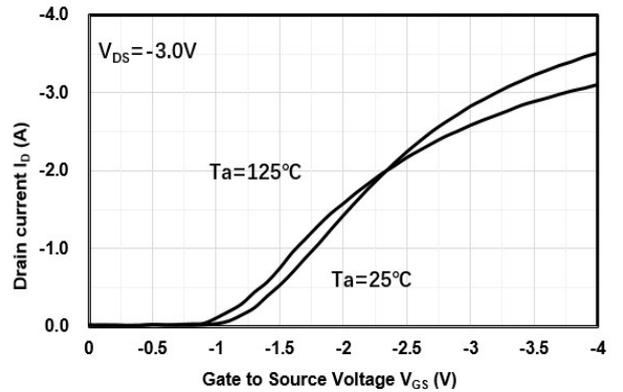


Figure2. Transfer Characteristics

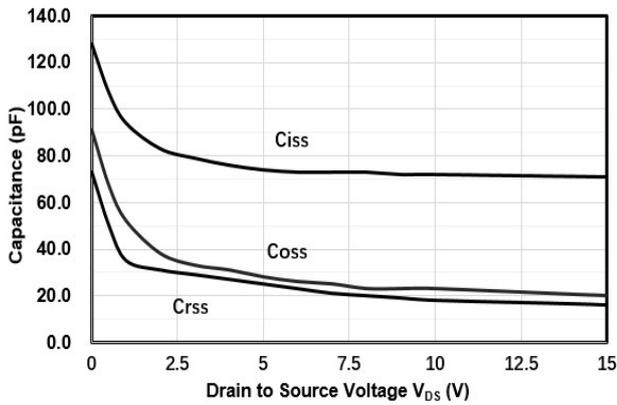


Figure3. Capacitance Characteristics

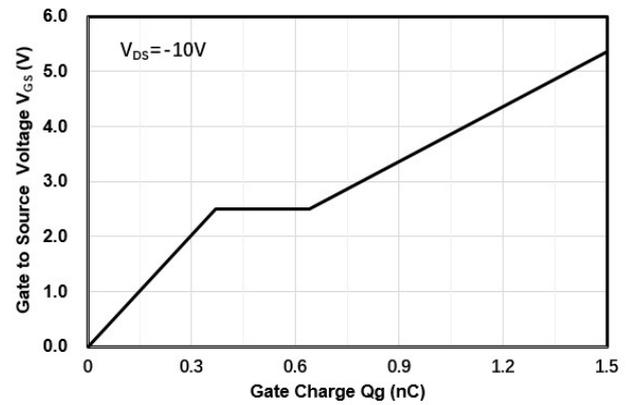


Figure4. Gate Charge

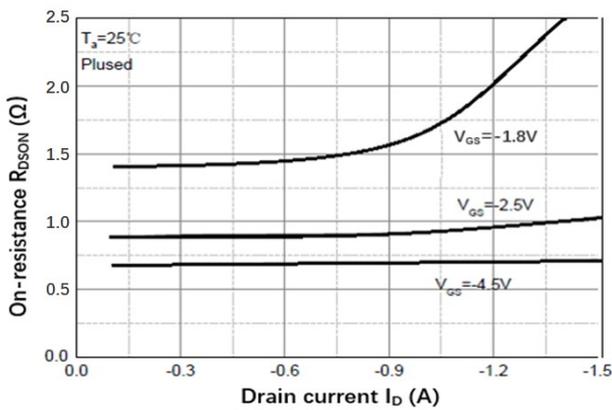


Figure5. Drain-Source on Resistance

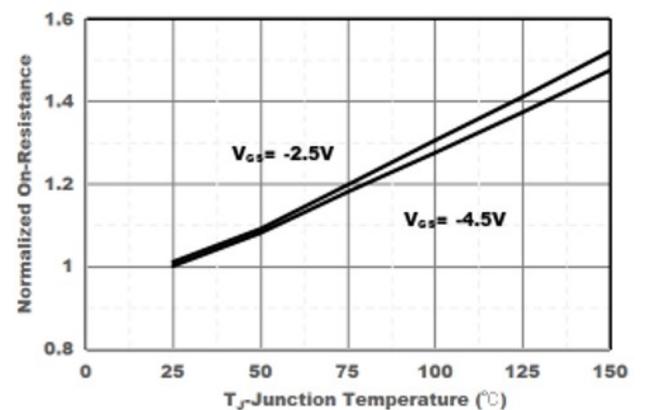


Figure6. Drain-Source on Resistance

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

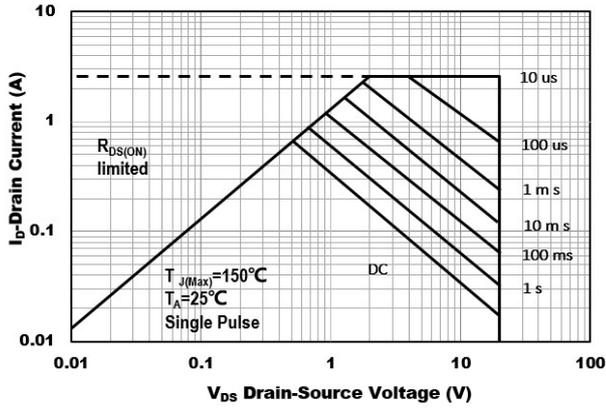


Figure7. Safe Operation Area

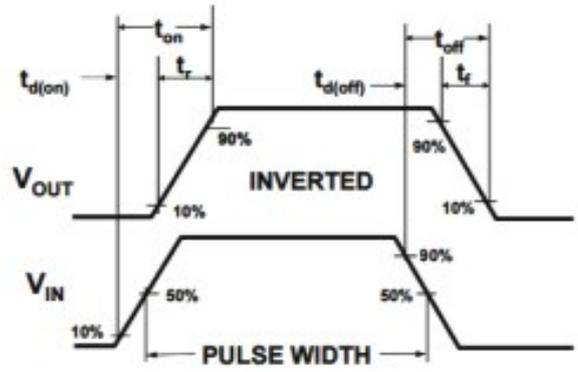
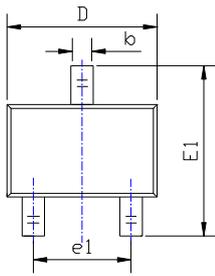
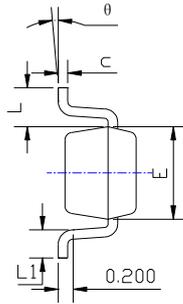


Figure8. Switching wave

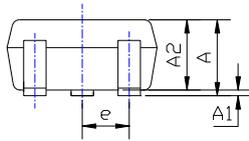
SOT323 PACKAGE INFORMATION



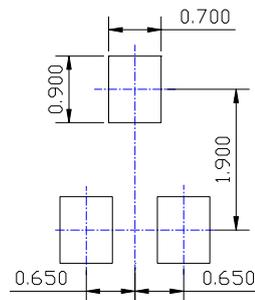
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT: mm

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.043	0.900	1.100
A1	0.000	0.004	0.000	0.100
A2	0.035	0.039	0.900	1.000
b	0.006	0.016	0.150	0.400
c	0.004	0.010	0.100	0.250
D	0.071	0.087	1.800	2.200
E	0.045	0.053	1.150	1.350
E1	0.085	0.096	2.150	2.450
e	0.026 TYP		0.650 TYP	
e1	0.047	0.055	1.200	1.400
L	0.021 REF		0.525 REF	
L1	0.010	0.018	0.260	0.460
theta	0°	8°	0°	8°

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.