HC3134KA

20V N-Channel MOSFET

General Description

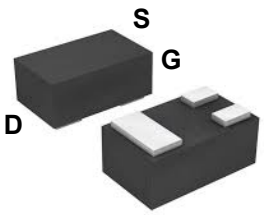
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

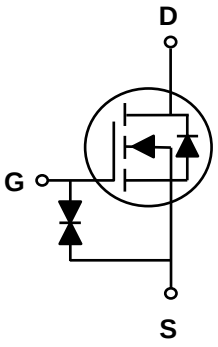
Features

V_{DS}	20V
I_D (at V_{GS}=4.5V)	0.7A
$R_{DS(ON)}$ (at V_{GS}=4.5V)	180mΩ(Typ)

ESD Protected Up to 2.0KV (HBM)

DFN1006-3L





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Drain Current-Continuous	TC=25°C	I_D	0.7	A
	TC=70°C	I_D	0.56	A
Drain Current – Pulsed		I_{DM}	2.8	A
Maximum Power Dissipation		P_D	0.9	W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	℃

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance junction-to-solder poin	$R_{\theta Jc}$		40	℃ /W
Thermal Resistance junction-to-Ambient	$R_{\theta JA}$		350	℃ /W

Electrical Characteristics (TJ=25℃ unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V,V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±10V,V_{DS}=0V			±10	μA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	0.3	0.7	1.2	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=4.5V, I_D=0.5A		180	300	mΩ
		V_{GS}=2.5V, I_D=0.4A		260	400	mΩ
		V_{GS}=1.8V, I_D=0.2A		420	700	mΩ
I_S	Maximum Body-Diode Continuous Current				0.7	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{DS}=10V,V_{GS}=0V, F=1.0MHz		56		pF
C_{oss}	Output Capacitance			20		pF
C_{rss}	Reverse Transfer Capacitance			2.5		pF
SWITCHING PARAMETERS						
$t_{d(on)}$	Turn-on Delay Time	V_{GS}=4.5V V_{DS}=10V R_G=25Ω I_D=0.5A		2		nS
t_r	Turn-on Rise Time			18.8		nS
$t_{d(off)}$	Turn-Off Delay Time			10		nS
t_f	Turn-Off Fall Time			23		nS
Q_g	Total Gate Charge	V_{DS}=10V,I_D=0.5A, V_{GS}=4.5V		1		nC
Q_{gs}	Gate-Source Charge			0.28		nC
Q_{gd}	Gate-Drain Charge			0.2		nC
V_{SD}	Diode Forward Voltage	V_{GS}=0V,I_{SD}=1A		0.70	1.3	V

Note：

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
3. Essentially independent of operating temperature.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

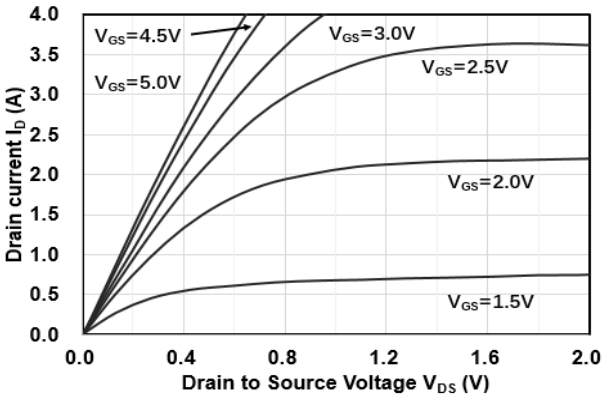


Figure1. Output Characteristics

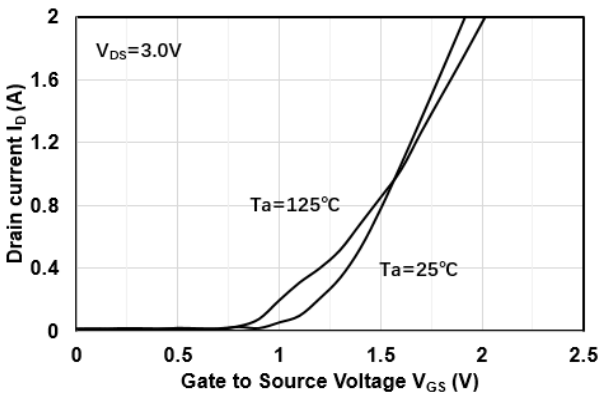


Figure2. Transfer Characteristics

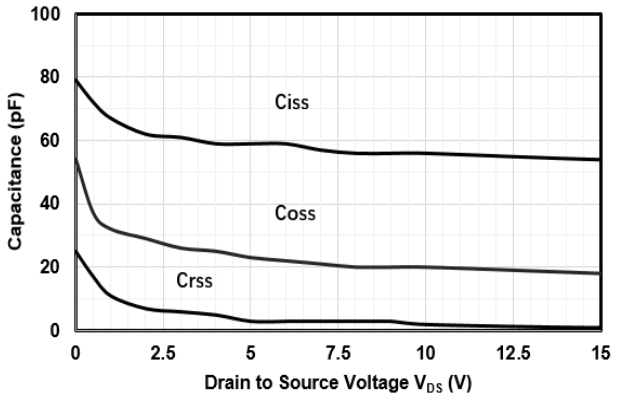


Figure3. Capacitance Characteristics

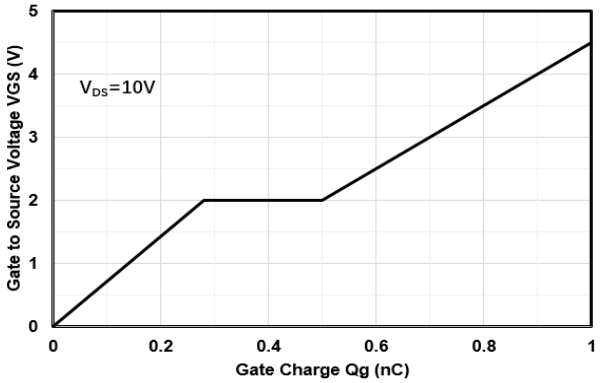


Figure4. Gate Charge

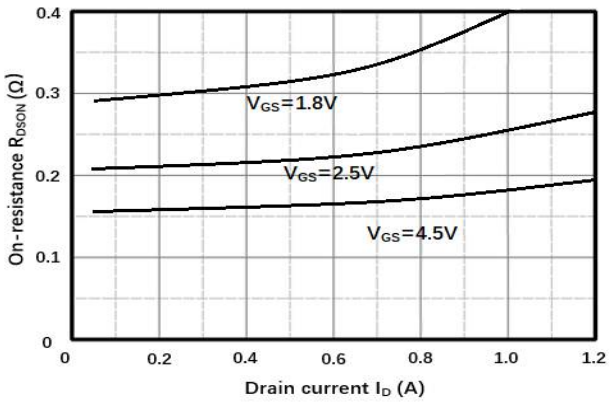


Figure5. Drain-Source on Resistance

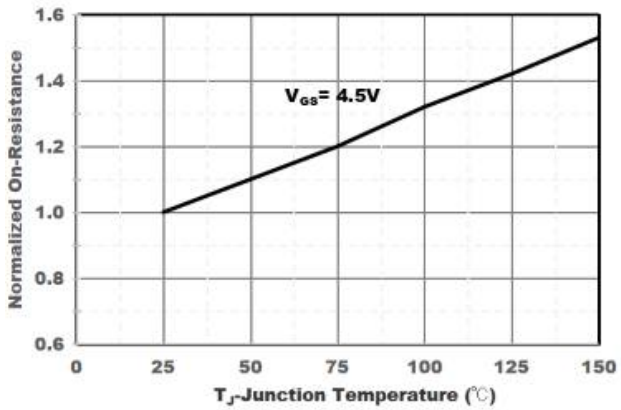


Figure6. Drain-Source on Resistance

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

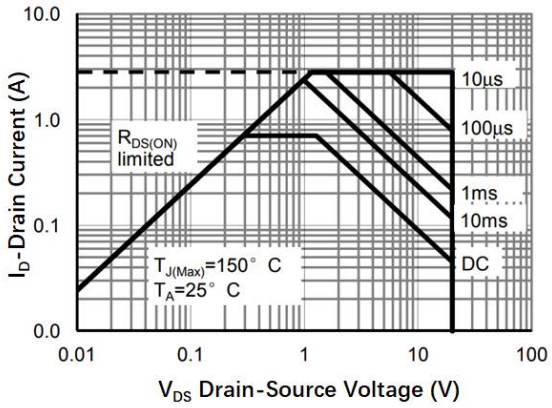


Figure7. Safe Operation Area

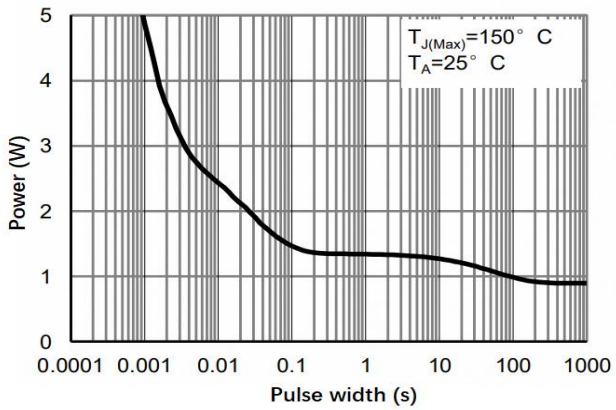


Figure8. Pulse Power Rating Junction-to-Ambient

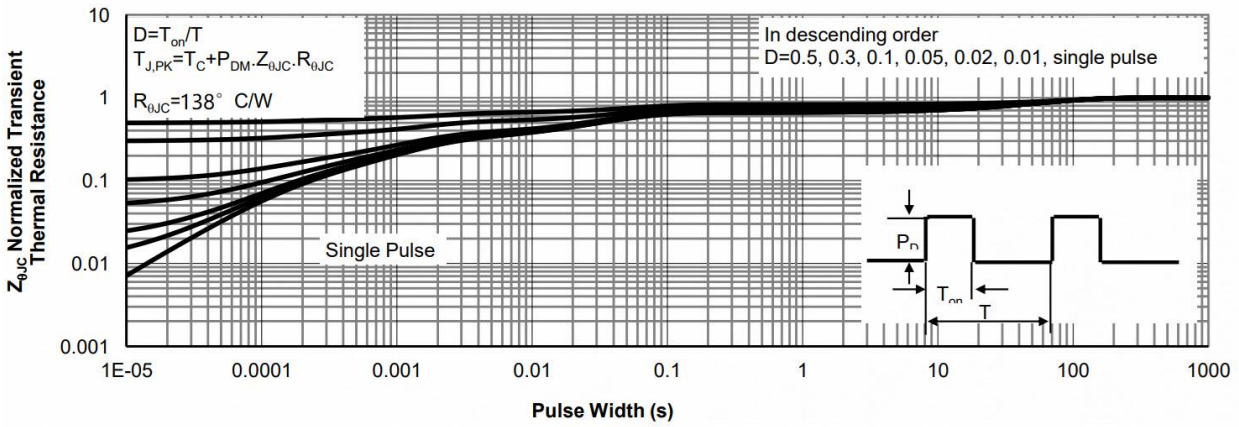
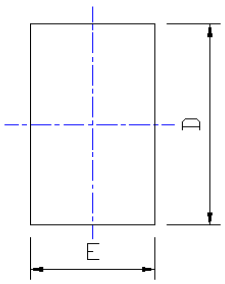
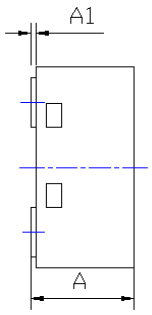


Figure9. Normalized Maximum Transient Thermal Impedance

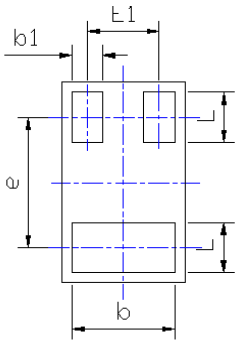
■DFN1006-3L Package information



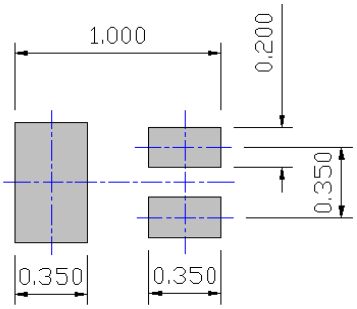
TOP VIEW



SIDE VIEW



BOTTOM VIEW



UNIT：mm

SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS			
SYMBOL	Millimeter		
	MIN.	NOM.	MAX.
A	0.42	---	0.55
A1	0.025REF		
b	0.45	0.50	0.55
b1	0.10	0.15	0.20
D	0.95	1.00	1.05
E	0.55	0.60	0.65
E1	0.35BSC		
e	0.65BSC		
L	0.20	0.25	0.30

NOTE:
1.PACKAGE BODY SIZES EXCLUDE LEAD BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.