

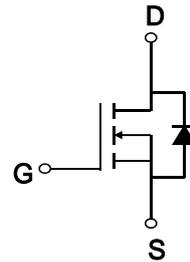
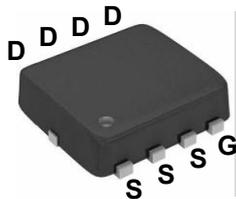
General Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features

V_{DS}	60V
I_D (at $V_{GS}=10V$)	30A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	17m Ω (Typ)

PDFN3*3



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units	
Drain-Source Voltage	V_{DS}	60	V	
Gate-Source Voltage	V_{GS}	± 20	V	
Drain Current-Continuous	TC=25 $^\circ\text{C}$	I_D	30	A
	TC=100 $^\circ\text{C}$	I_D	18	A
Maximum Power Dissipation	P_D	31	W	
Drain Current - Pulsed	I_{DM}	90	A	
Single pulse avalanche energy	E_{AS}	38	mJ	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ\text{C}$	

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance junction-case	$R_{\theta Jc}$		3.7	$^\circ\text{C/W}$
Thermal Resistance junction-to-Ambient	$R_{\theta JA}$		62	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=60V, V_{GS}=0V$			1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=20V, V_{DS}=0V$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.6	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=15A$		17	21	m Ω
		$V_{GS}=4.5V, I_D=10A$		22	28	m Ω
DYNAMIC PARAMETERS						
C_{ISS}	Input Capacitance	$V_{DS}=30V, V_{GS}=0V,$ $F=1.0MHz$		1115		pF
C_{OSS}	Output Capacitance			91		pF
C_{RSS}	Reverse Transfer Capacitance			82		pF
SWITCHING PARAMETERS						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=30V, I_D=1A,$ $V_{GS}=10V,$ $R_G=3.3\Omega$		5.9		nS
t_r	Turn-on Rise Time			9.1		nS
$t_{d(off)}$	Turn-Off Delay Time			35		nS
t_f	Turn-Off Fall Time			12		nS
Q_g	Total Gate Charge	$V_{DS}=30V, I_D=12A,$ $V_{GS}=10V$		27		nC
Q_{gs}	Gate-Source Charge			2.9		nC
Q_{gd}	Gate-Drain Charge			7.6		nC
V_{SD}	Diode Forward Voltage	$V_{GS}=0V, I_{SD}=1A$		0.72	1.3	V

Note:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. $V_{DD}=50V, L=0.3mH, I_{AS}=15A.,$ Starting T_J=25°C
3. The data tested by pulsed , pulse width $\cong 30\mu s$, duty cycle $\cong 2\%$.
4. Essentially independent of operating temperature.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

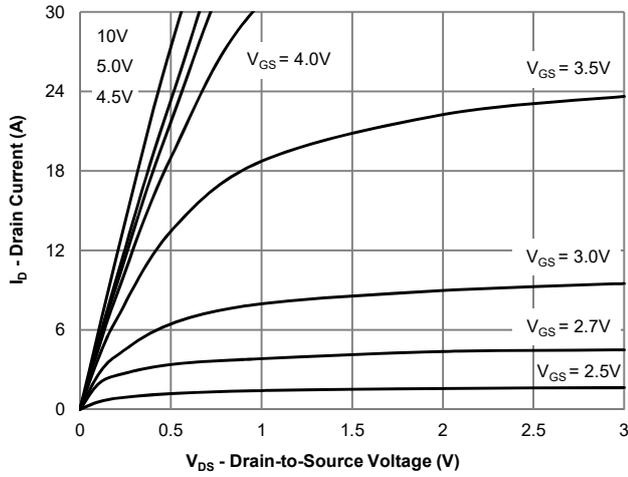


Figure 1: Output Characteristics

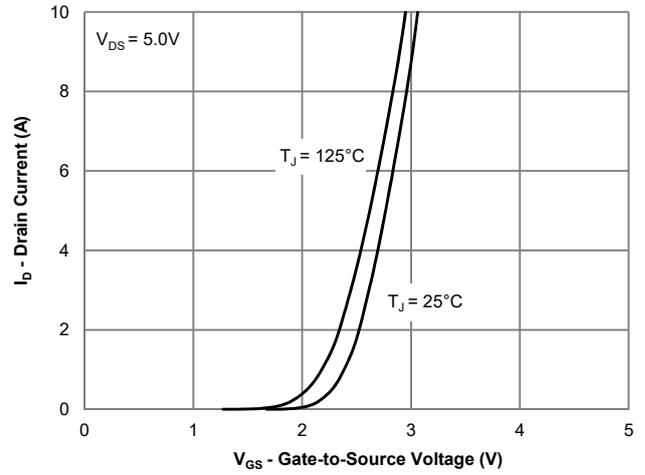


Figure 2: Transfer Characteristics

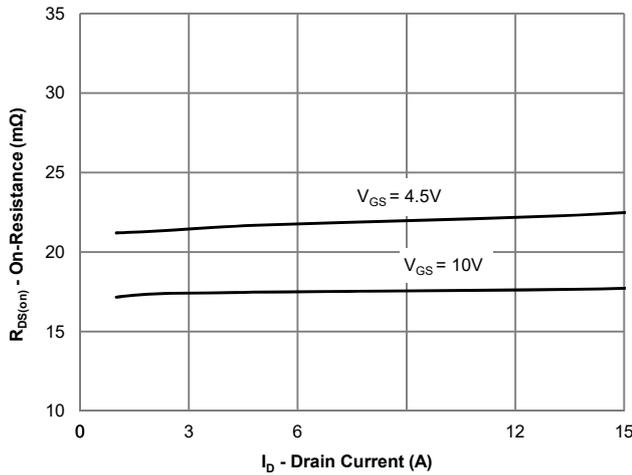


Figure 3: On-Resistance vs. Gate-Source Voltage

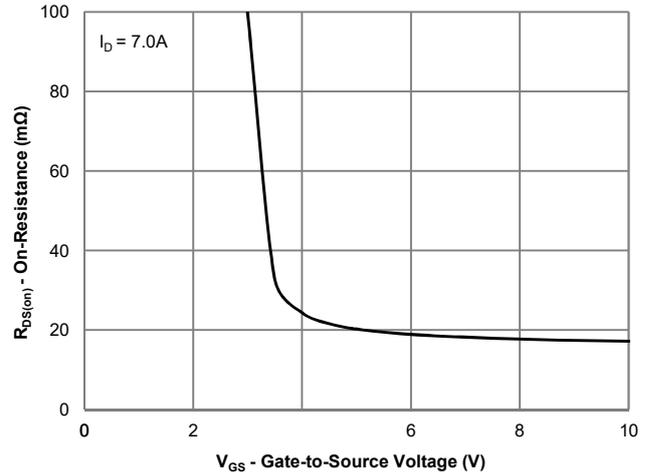


Figure 4: On-Resistance vs. Gate-Source Voltage

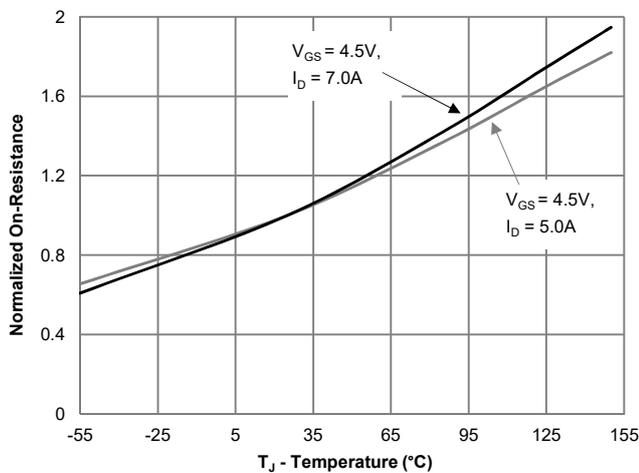


Figure 5: On-Resistance vs. Junction Temperature

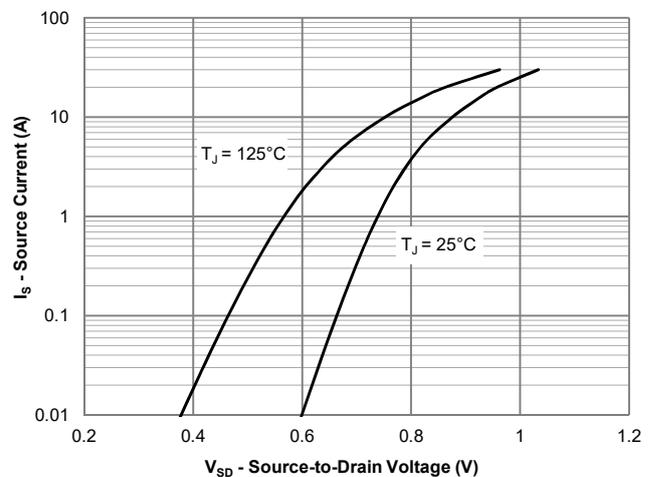


Figure 6: Source-Drain Diode Forward Voltage

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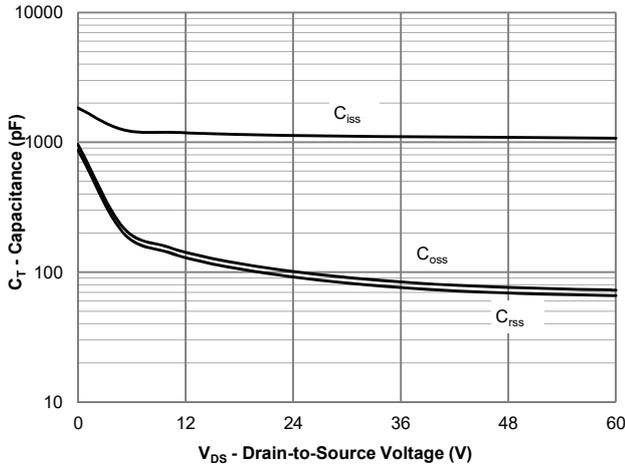


Figure 7: Capacitance Characteristics

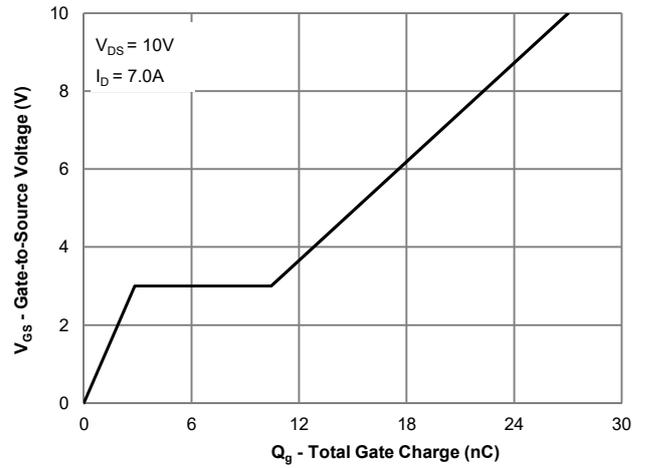


Figure 8: Gate Charge Characteristics

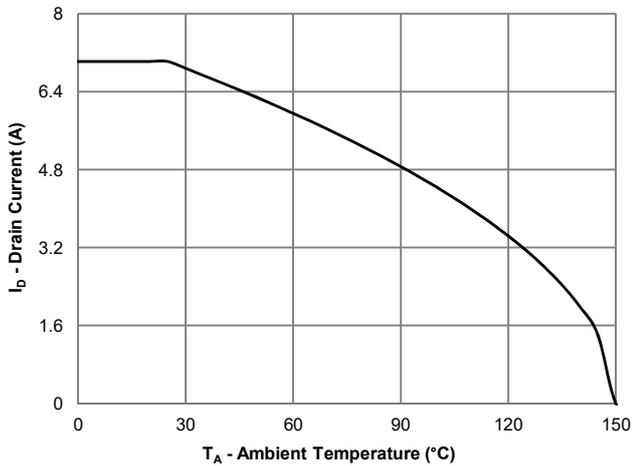


Figure 9: Current Derating

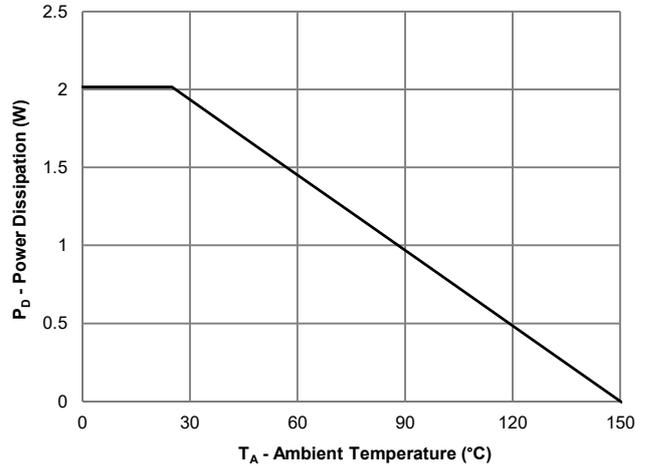


Figure 10: Power Derating

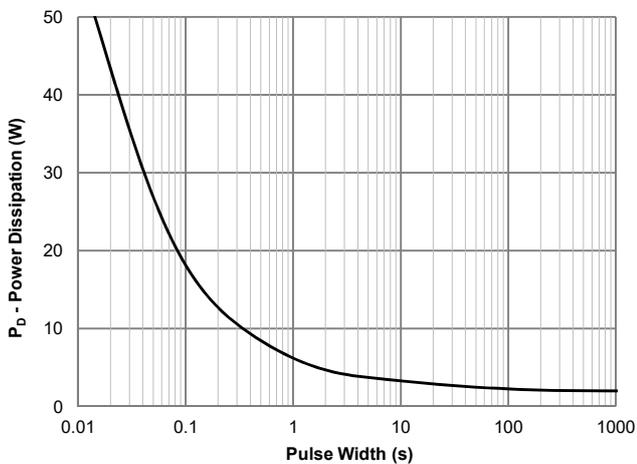


Figure 11: Single Pulse Power, Junction-to-Ambient

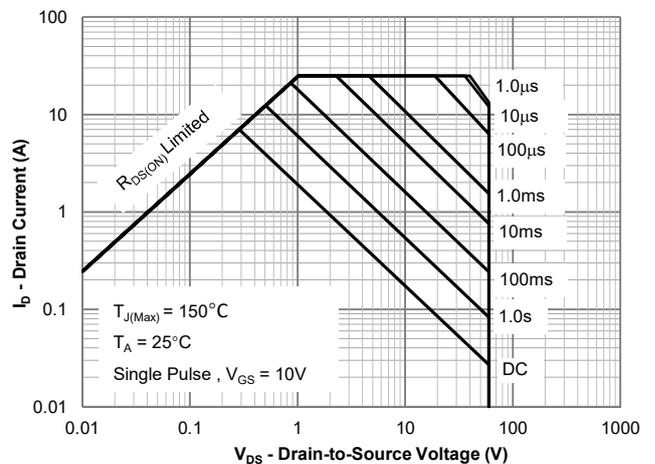


Figure 12: Safe Operating Area

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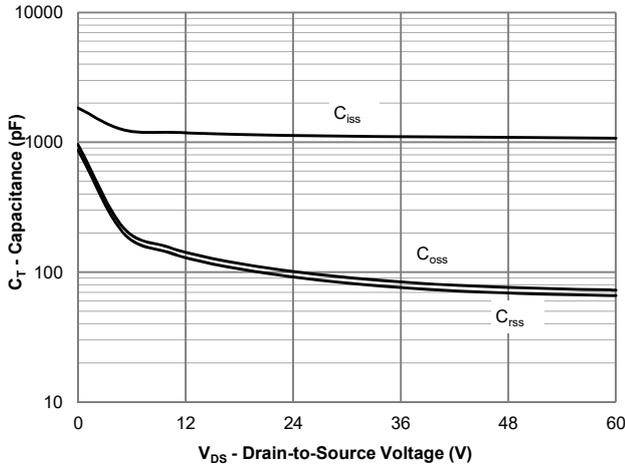


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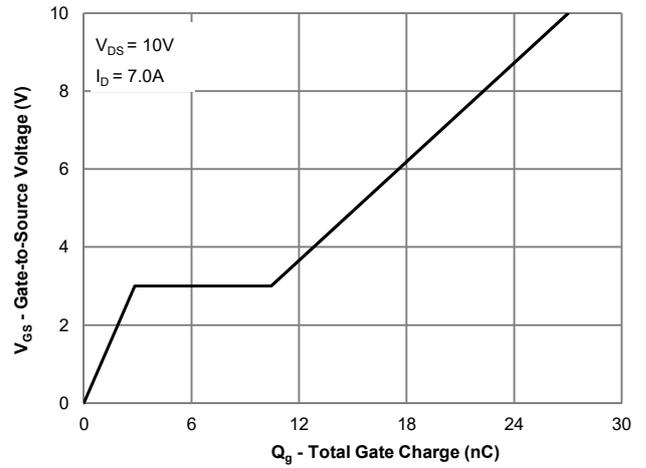


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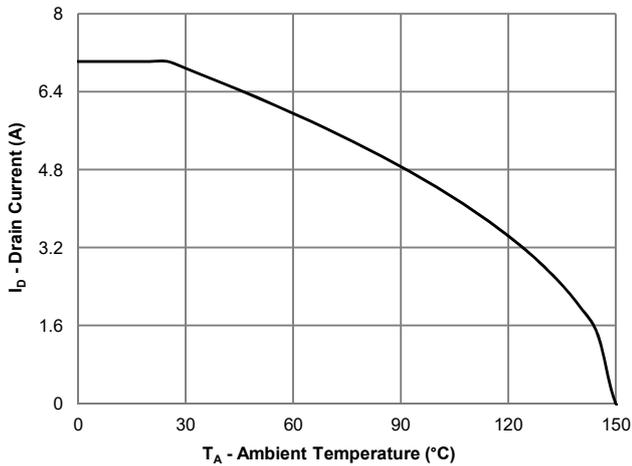


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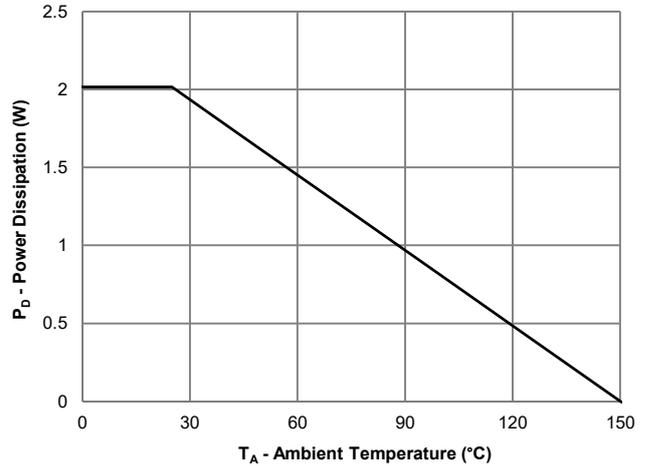


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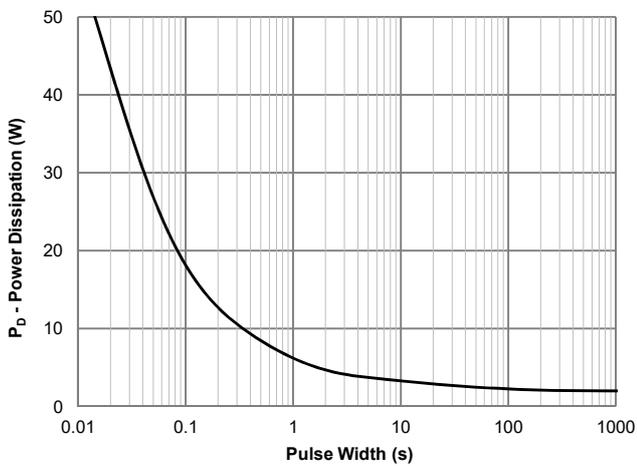


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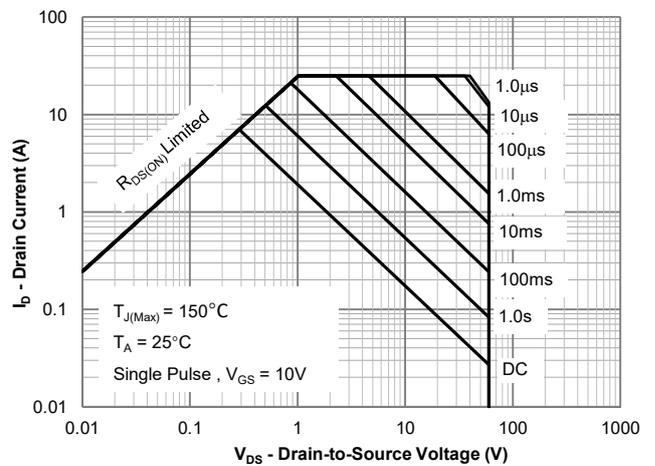


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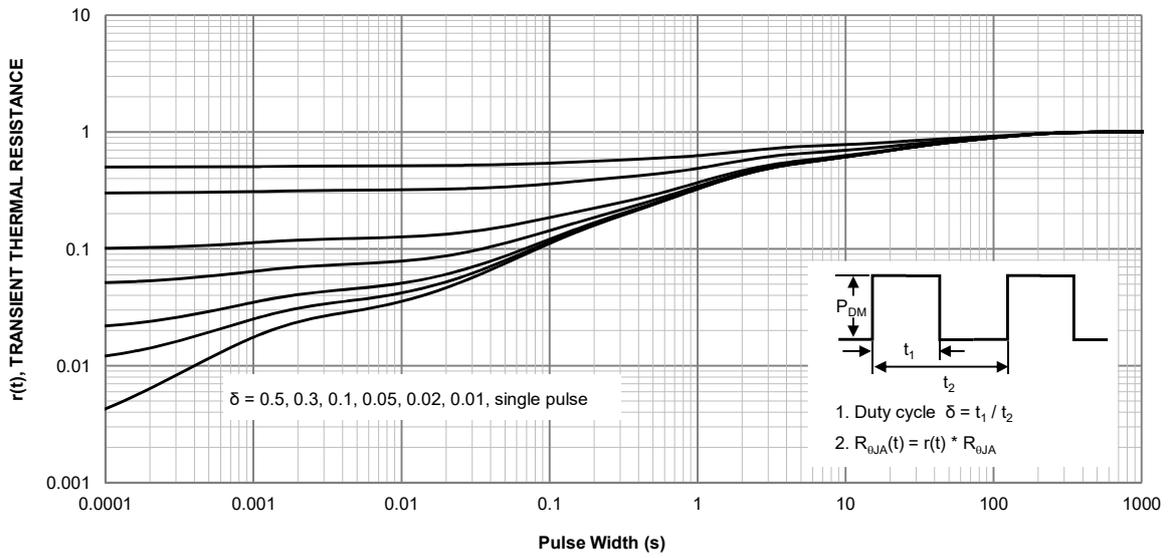
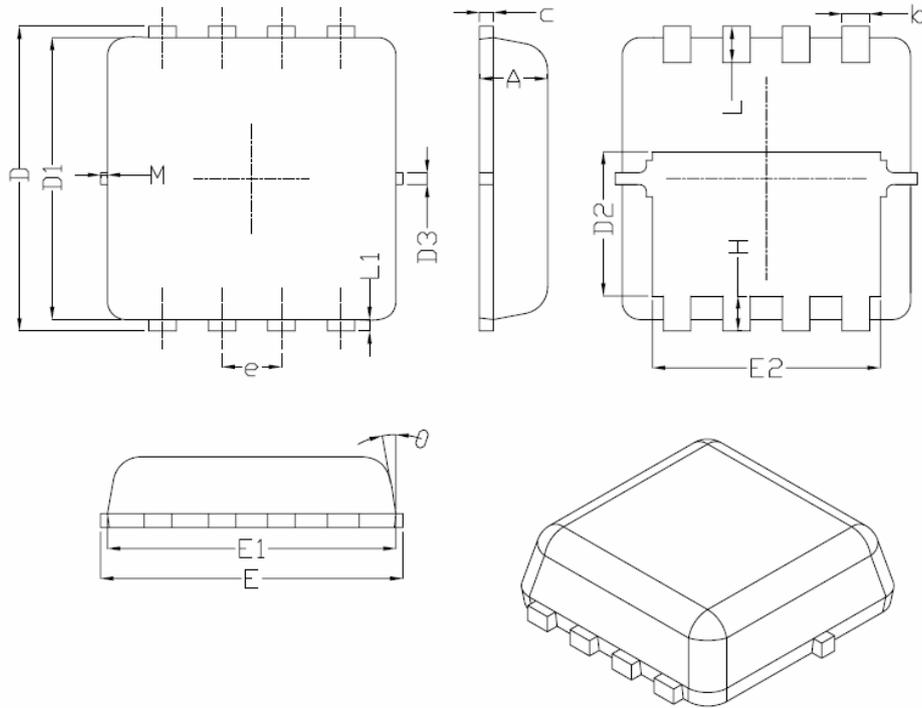


Figure 13: Normalized Thermal Transient Impedance

PDFN3*3 PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.48	1.58	1.68
D3	-	0.13	-
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BS		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	-	0.13	-
M	*	*	0.15
θ		10°	12°