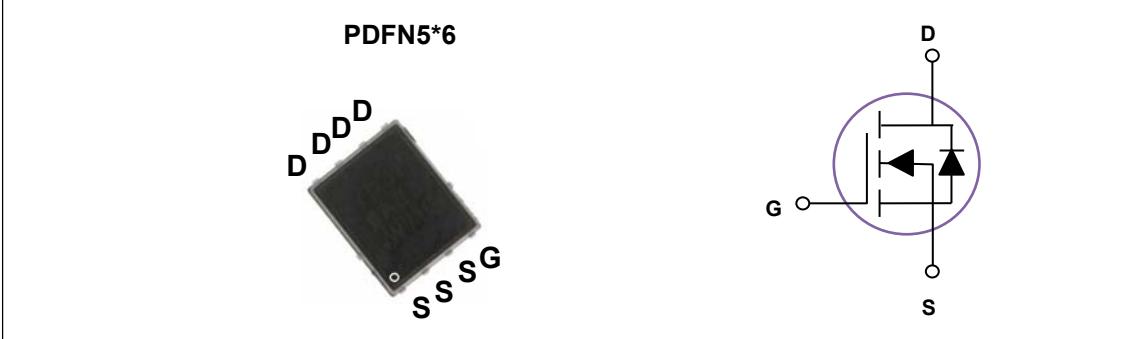


<b>General Description</b>	<b>Features</b>
<p>These N-Channel enhancement mode power field effect transistors are using SGT technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.</p>	<p> <math>V_{DS}</math> 100V  <math>I_D</math> (at <math>V_{GS}=10V</math>) 112A  <math>R_{DS(ON)}</math> (at <math>V_{GS}=10V</math>) 3.3mΩ(Typ)         </p>



<b>Absolute Maximum Ratings <math>T_A=25^\circ C</math> unless otherwise noted</b>				
<b>Parameter</b>	<b>Symbol</b>	<b>Maximum</b>	<b>Units</b>	
Drain-Source Voltage	$V_{DS}$	100	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V	
Drain Current-Continuous	$I_D$ (TC=25°C)	112	A	
	$I_D$ (TC=100°C)	71	A	
Maximum Power Dissipation	$P_D$	104	W	
Single pulse avalanche energy <sup>(1)</sup>	$E_{AS}$	231	mJ	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	°C	
<b>Thermal Characteristics</b>				
<b>Parameter</b>	<b>Symbol</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>
Thermal Resistance junction-case	$R_{\theta JC}$		1.2	°C /W
Thermal Resistance unction-to-Ambient	$R_{\theta JA}$		65	°C /W

## Electrical Characteristics (TJ=25°C unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=80V, V_{GS}=0V$			1	$\mu A$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	3.0	4.0	V
$R_{DS(ON)}$	Drain-Source On-State resistance	$V_{GS}=10V, I_D=20A$		3.3	4.2	$m\Omega$
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=50V, V_{GS}=0V$ , F=1.0MHz		3434		pF
$C_{oss}$	Output Capacitance			906		pF
$C_{rss}$	Reverse Transfer Capacitance			14		pF
<b>SWITCHING PARAMETERS</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=40V, I_D=1A$ , $V_{GS}=10V$ , $R_G=6\Omega$		15		nS
$t_r$	Turn-on Rise Time			34		nS
$t_{d(off)}$	Turn-Off Delay Time			60		nS
$t_f$	Turn-Off Fall Time			50		nS
$Q_g$	Total Gate Charge	$V_{DS}=40V, I_D=10A$ , $V_{GS}=10V$		57		nC
$Q_{gs}$	Gate-Source Charge			11		nC
$Q_{gd}$	Gate-Drain Charge			16		nC
$V_{SD}$	Diode Forward Voltage	$V_{GS}=0V, I_{SD}=1A$		0.72	1.4	V

## Note:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2.  $V_{DD}=50V, V_{GS}=10V, L=0.1mH, I_{AS}=60A$ , Starting TJ=25°C.
3. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$ .
4. Essentially independent of operating temperature.

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

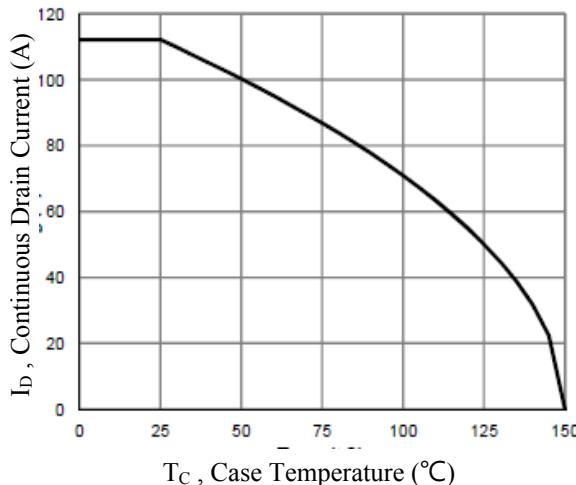
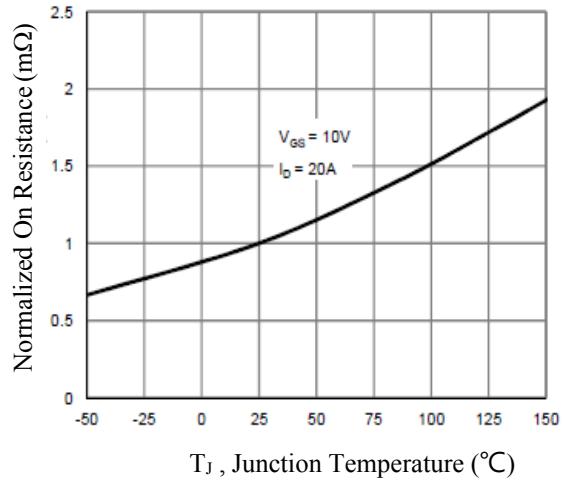
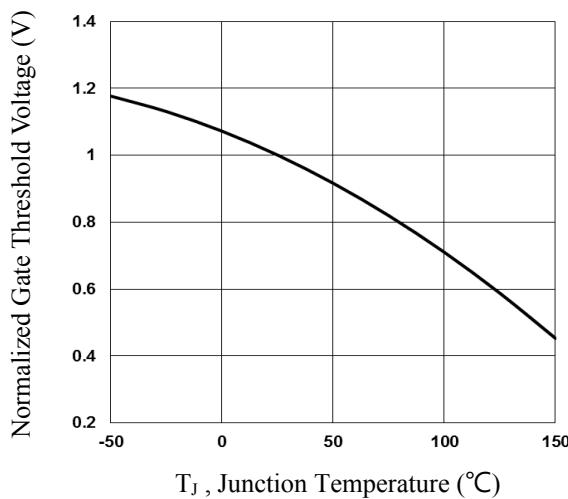
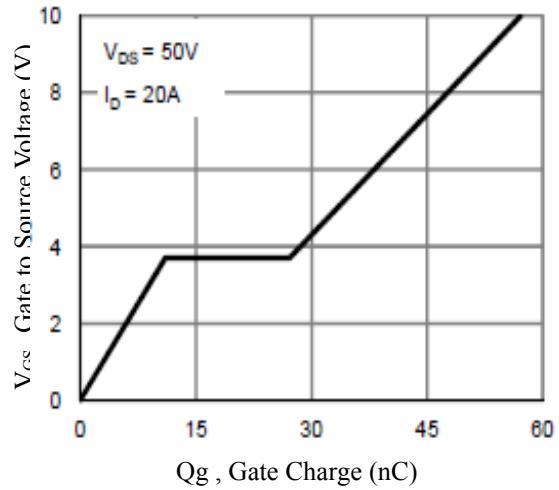
Fig.1 Continuous Drain Current vs.  $T_C$ Fig.2 Normalized RDSON vs.  $T_J$ Fig.3 Normalized  $V_{th}$  vs.  $T_J$ 

Fig.4 Gate Charge Characteristics

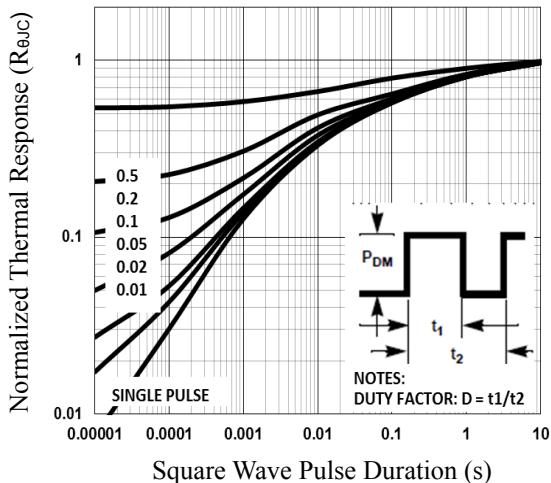


Fig.5 Normalized Transient Impedance

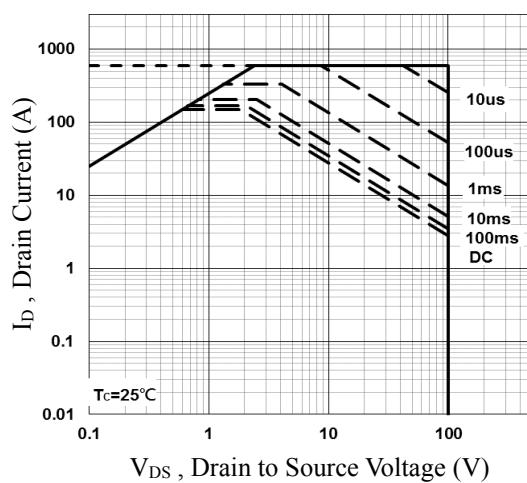


Fig.6 Maximum Safe Operation Area

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

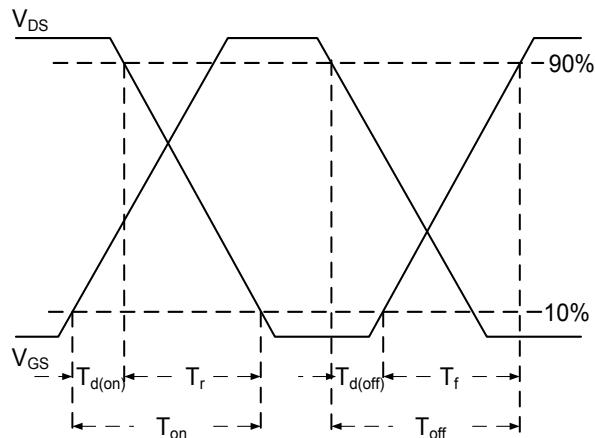


Fig.7 Switching Time Waveform

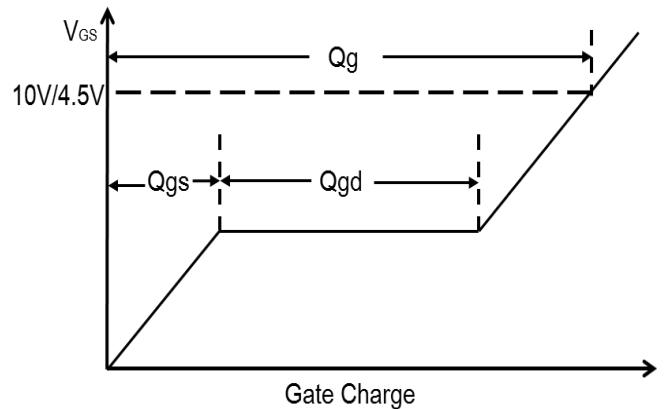
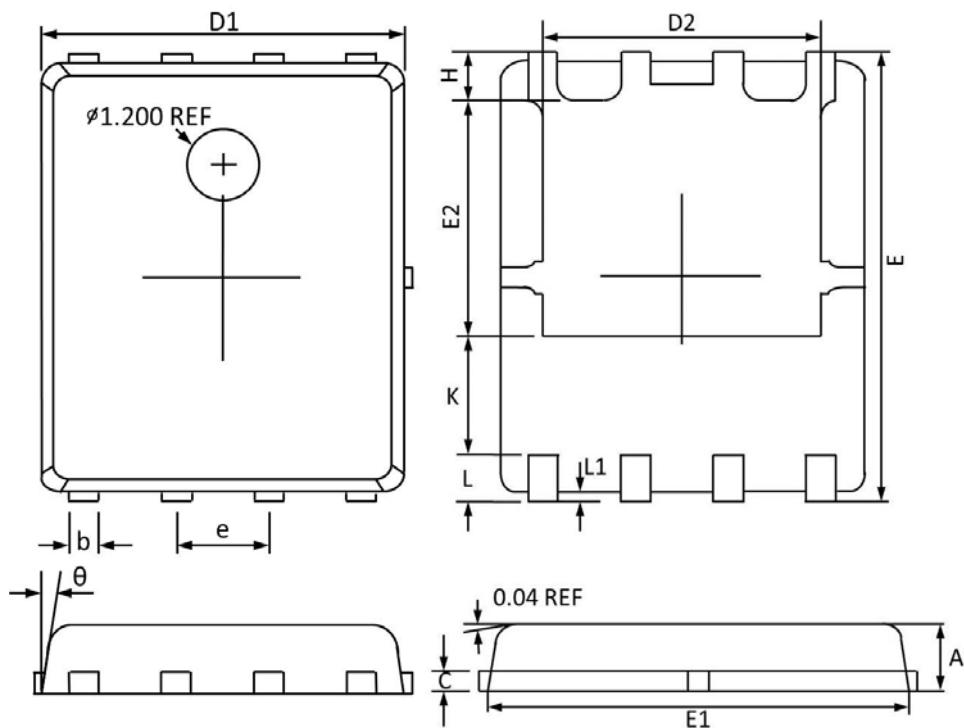


Fig.8 Gate Charge Waveform

## PDFN5\*6 PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MAX	MIN	MAX	MIN
A	1.100	0.800	0.043	0.031
b	0.510	0.330	0.020	0.013
C	0.300	0.200	0.012	0.008
D1	5.100	4.800	0.201	0.189
D2	4.100	3.610	0.161	0.142
E	6.200	5.900	0.244	0.232
E1	5.900	5.700	0.232	0.224
E2	3.780	3.350	0.149	0.132
e	1.27BSC		0.05BSC	
H	0.700	0.410	0.028	0.016
K	1.500	1.100	0.059	0.043
L	0.710	0.510	0.028	0.020
L1	0.200	0.060	0.008	0.002
$\theta$	12°	0°	12°	0°